

FIG. 1

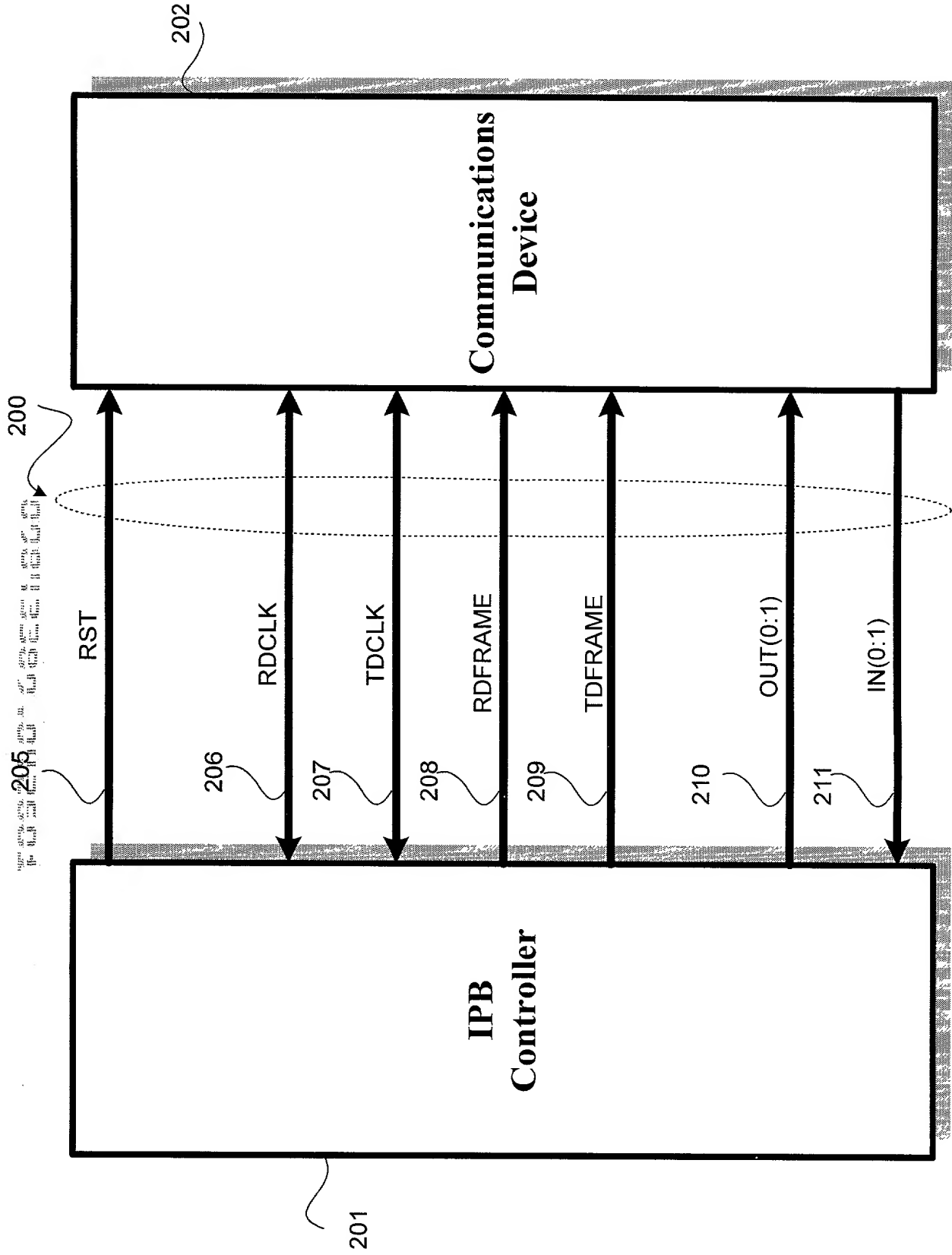


FIG. 2a

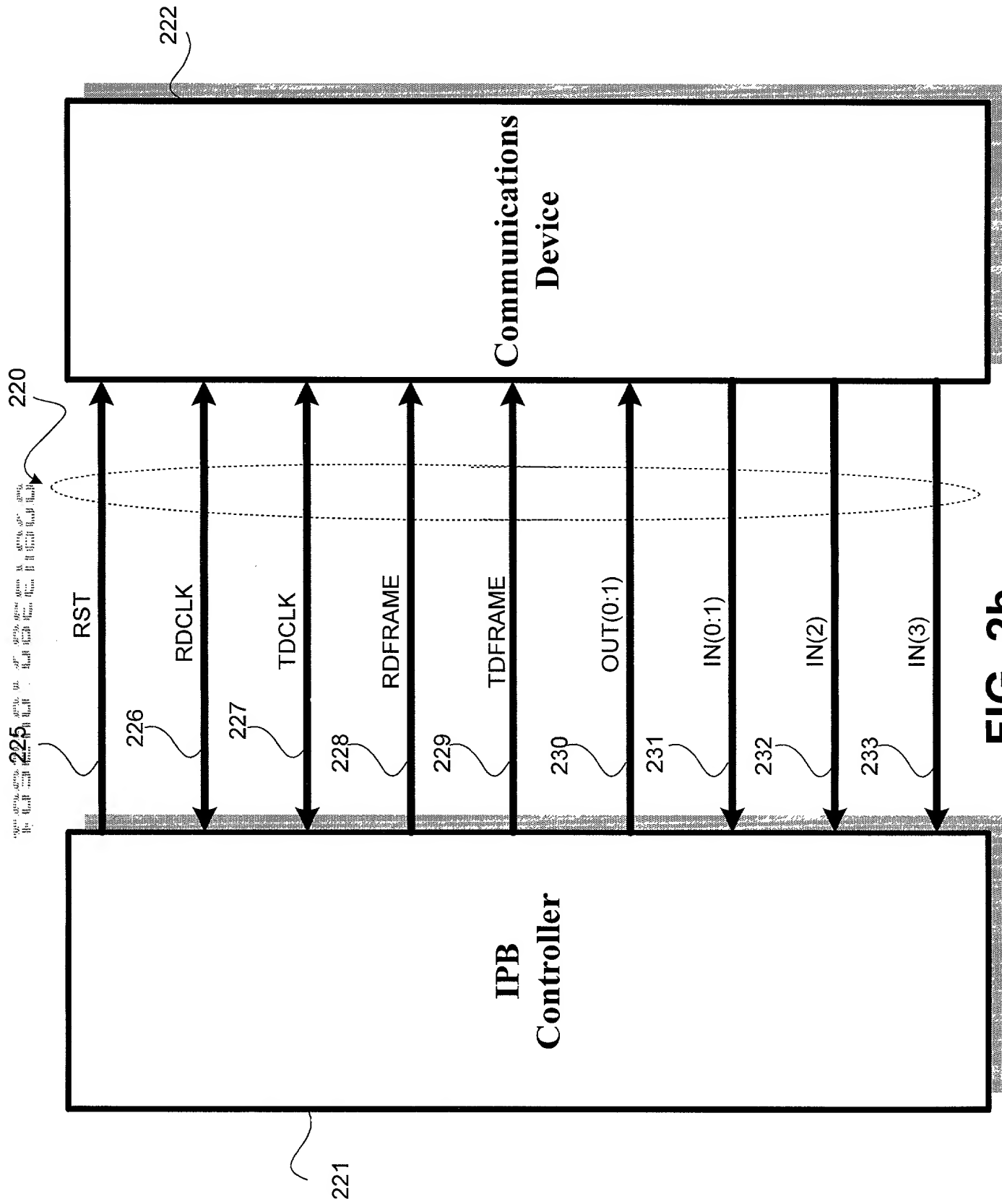


FIG. 2b

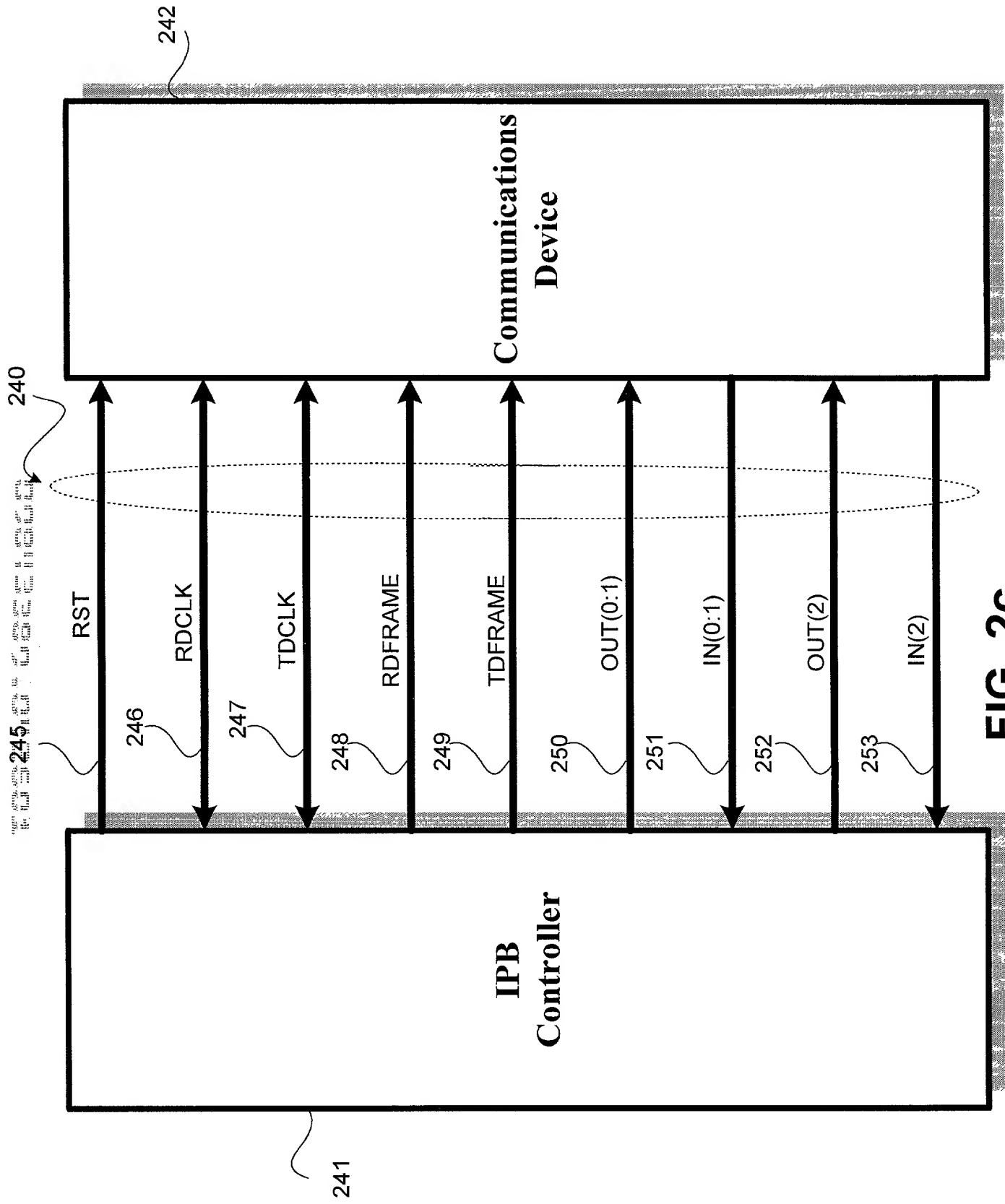


FIG. 2c

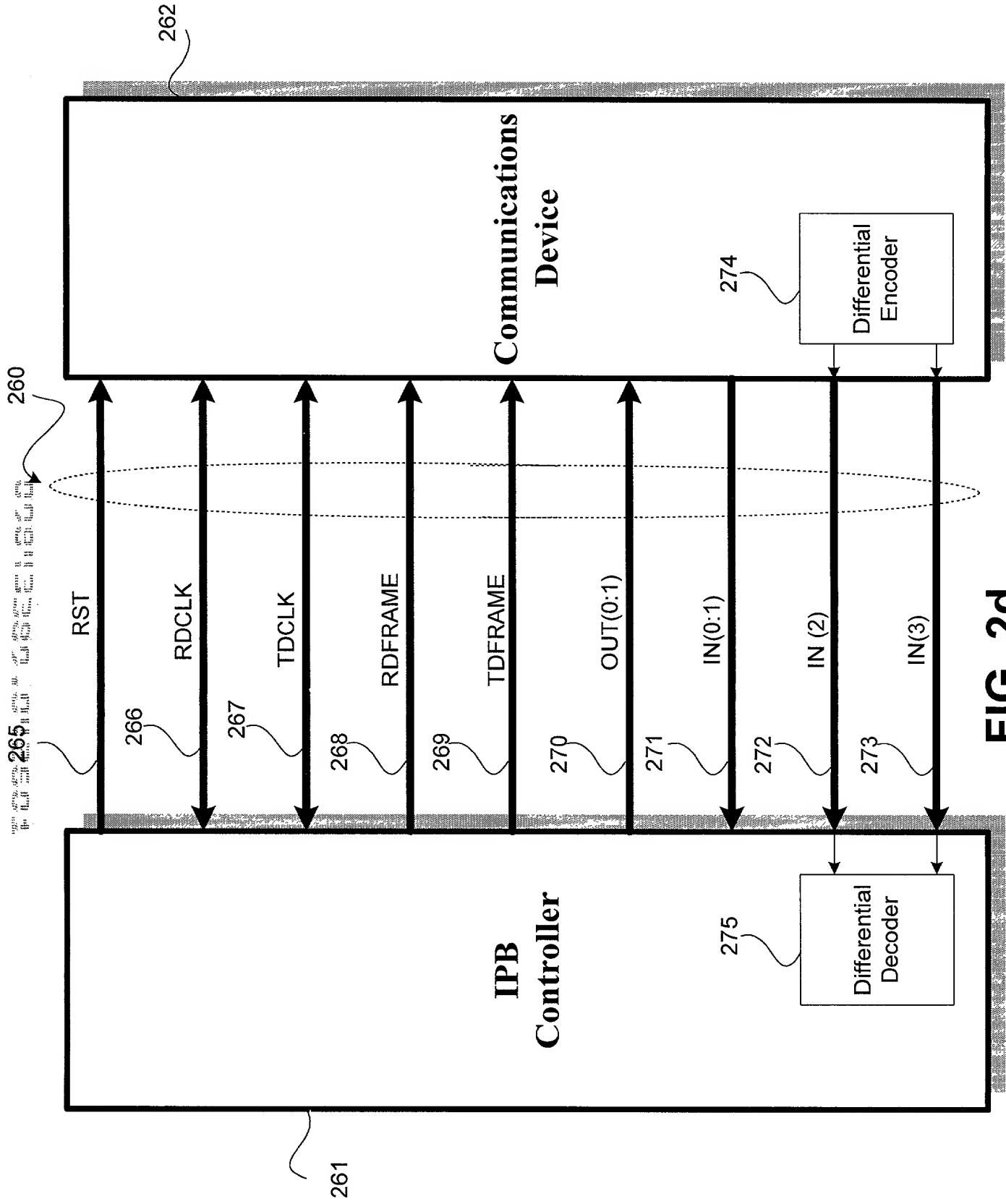


FIG. 2d

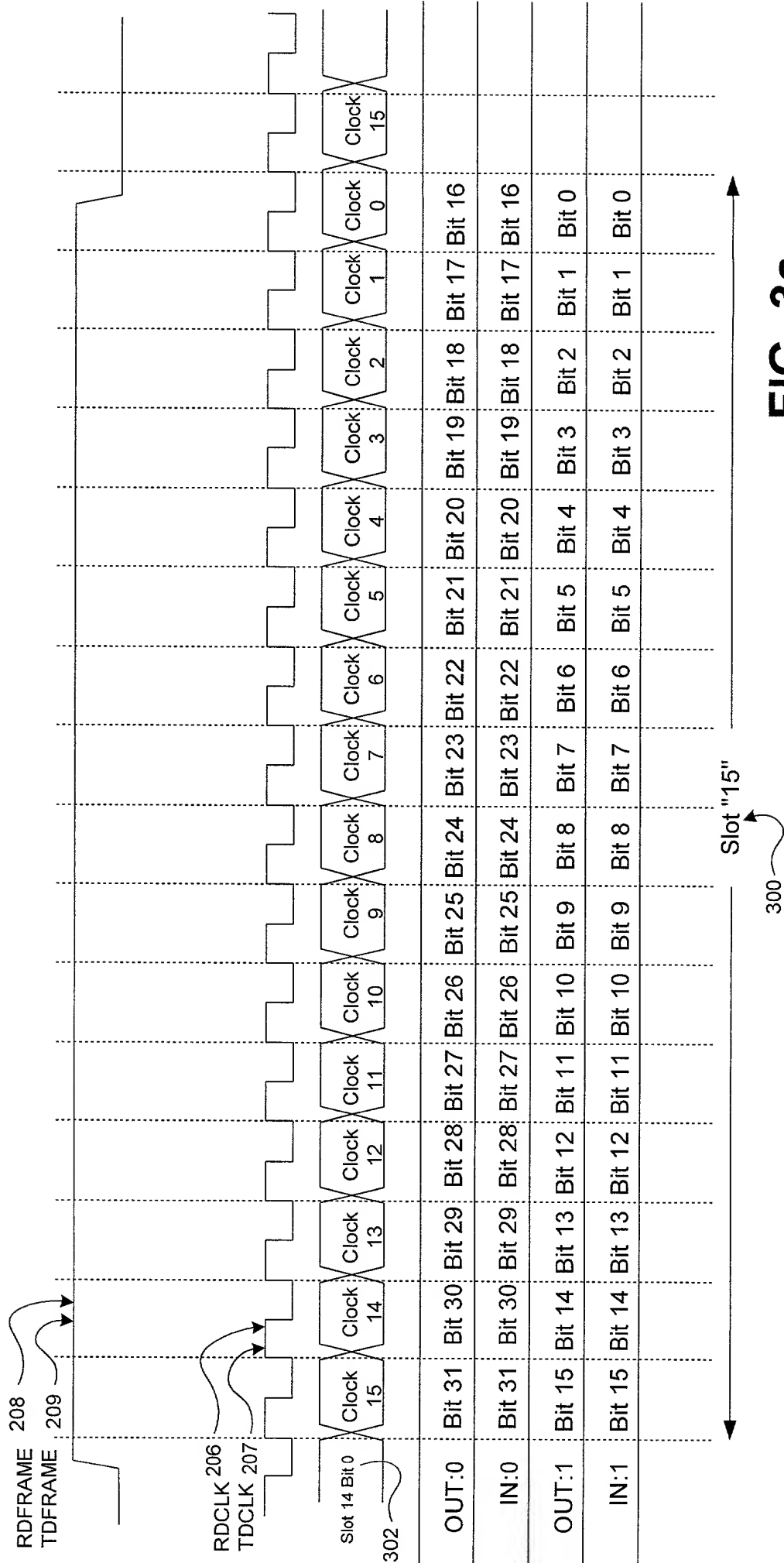


FIG. 3a

FIG. 3b is a timing diagram illustrating the relationship between the RDCLK 206 and TDCLK 207 signals and the data transfer process. The diagram shows the RDCLK 206 and TDCLK 207 signals, the RDFRAME 208 and TDFRAME 209 signals, and the data transfer process across 16 clock cycles. The data transfer process is divided into three sections: OUT:0, IN:0, and IN:1. The OUT:0 section shows data transfer from the device to the host, and the IN:0 and IN:1 sections show data transfer from the host to the device. The diagram also shows the relationship between the RDCLK 206 and TDCLK 207 signals and the data transfer process.

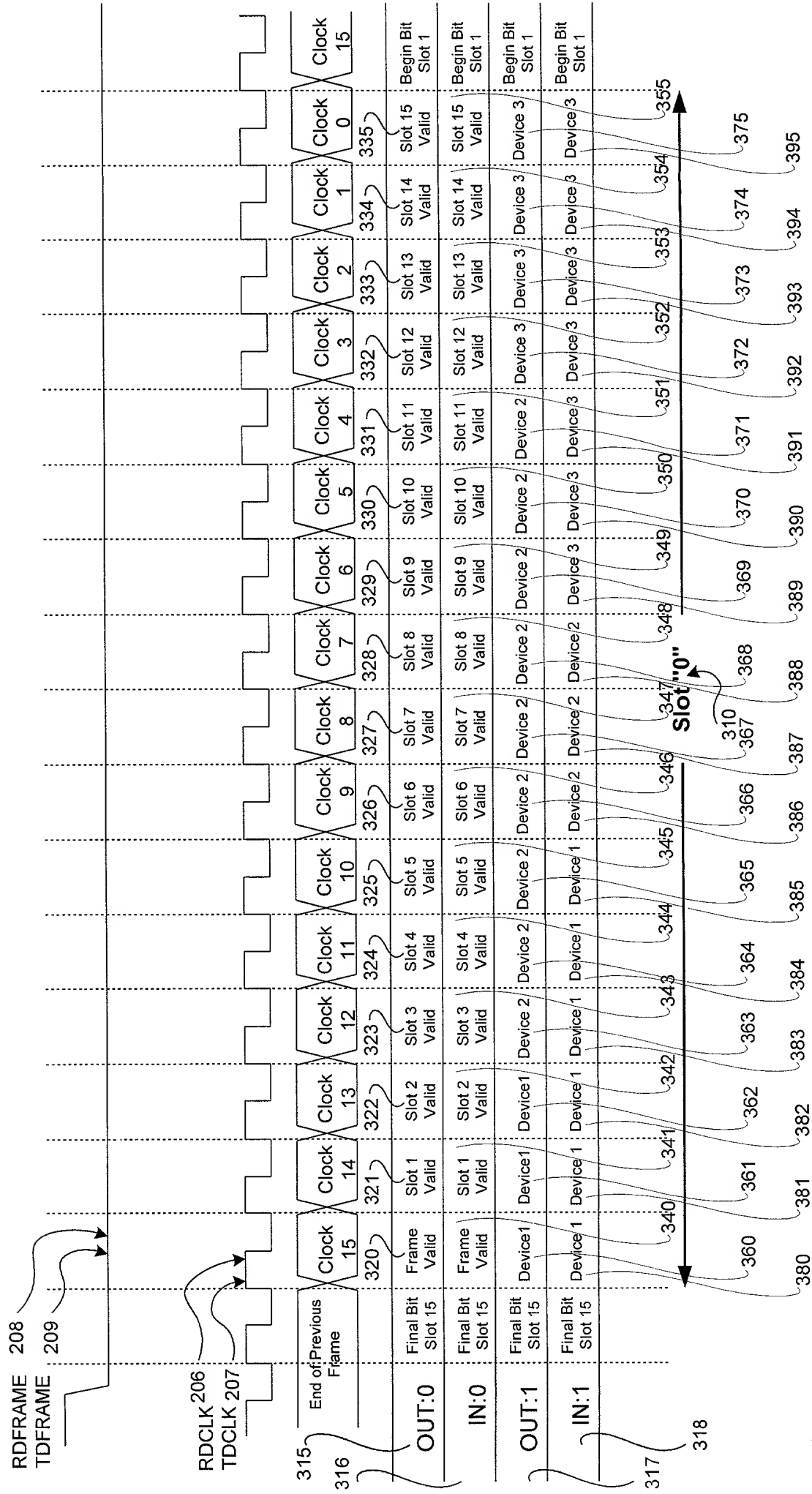


FIG. 3b

FIG. 3C is a timing diagram illustrating the relationship between the RDCLK 226, TDCLK 227, and the data bits OUT:0, IN:0, OUT:1, IN:1, IN:2, and IN:3. The diagram shows that the data bits are sampled on the rising edge of the RDCLK 226 and the data bits are driven on the rising edge of the TDCLK 227. The data bits are organized into slots of 15 bits each, with a total of 3000 bits per slot.

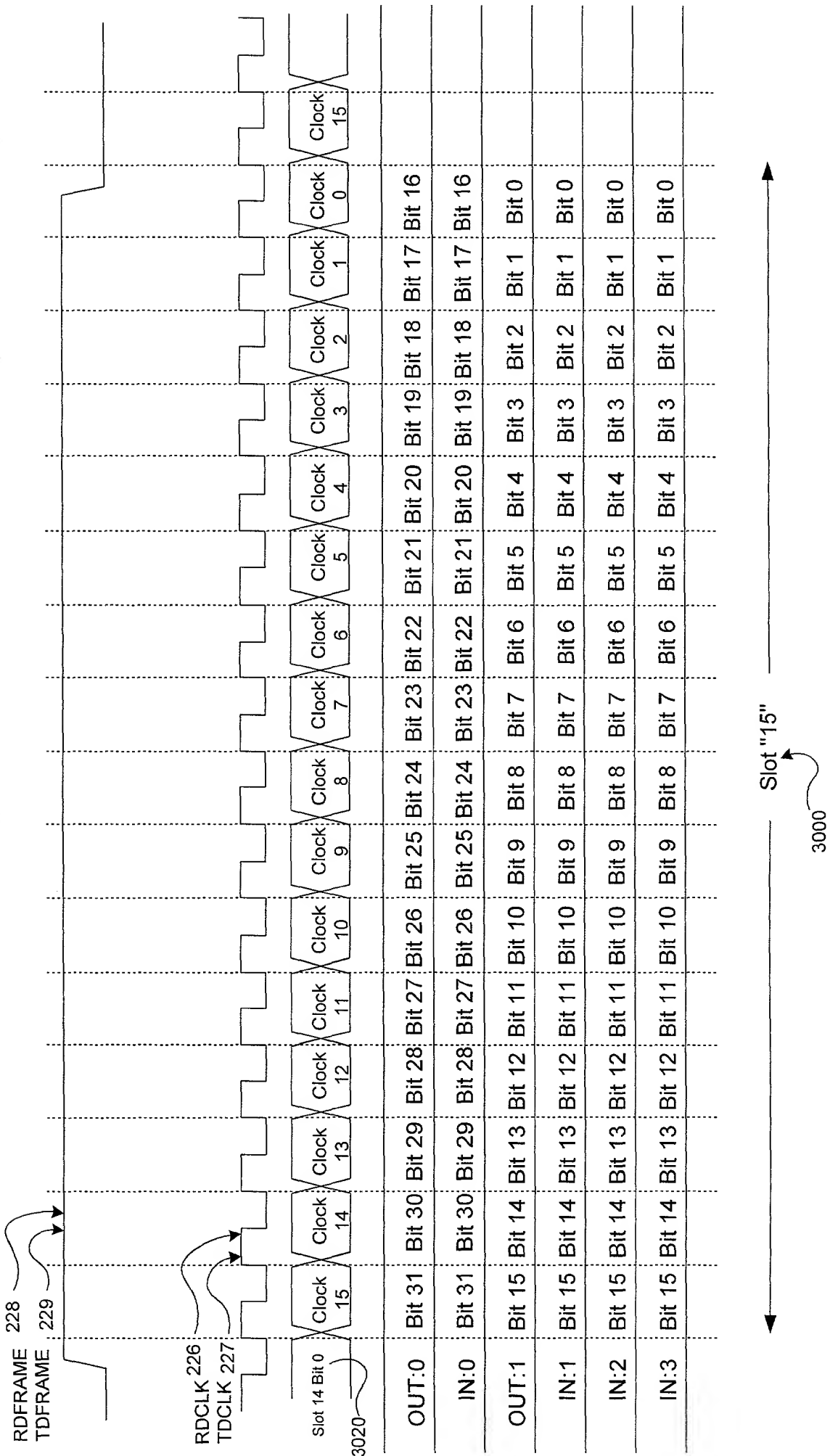


FIG. 3C

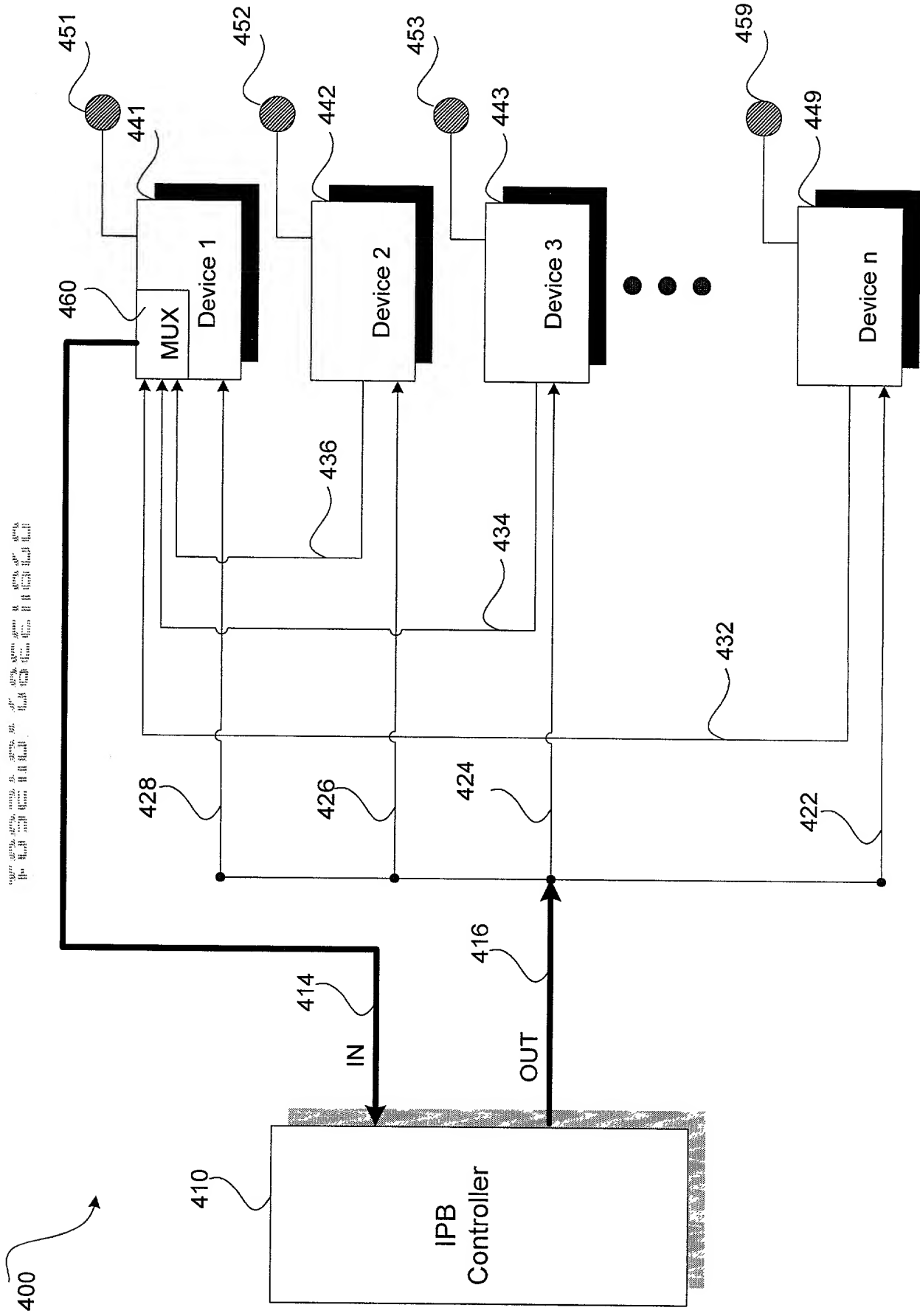


FIG. 4

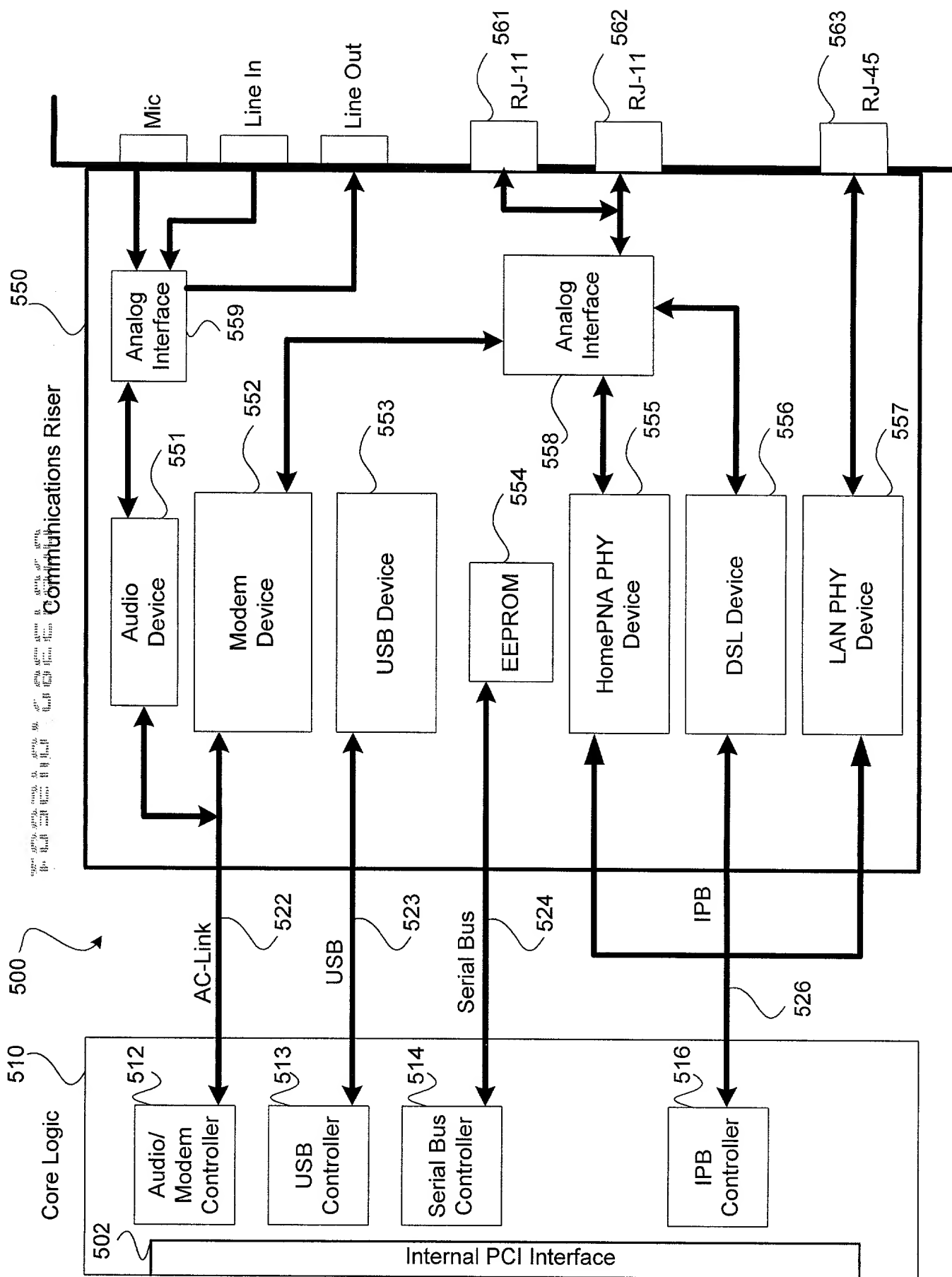


FIG. 5